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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/882,760	06/15/2001	Shuo-Yen Robert Li	Li7	1794

7590 01/11/2005

John T. Peoples
14 Blue Jay Court
Warren, NJ 07059

EXAMINER	
LEE, ANDREW CHUNG CHEUNG	

ART UNIT	PAPER NUMBER
2664	

DATE MAILED: 01/11/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/882,760	LI ET AL.	
	Examiner	Art Unit	
	Andrew C Lee	2664	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *15 June 2001*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1 -24* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1 - 24* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☒ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☒ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *06/15/2001*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Drawings

1. The drawings are objected to as failing to comply with 37 CFR 1.84(p)(5) because they include the following reference character(s) not mentioned in the description: Fig.1, the referenced elements " 116, 141". Corrected drawing sheets in compliance with 37 CFR 1.121(d), or amendment to the specification to add the reference character(s) in the description in compliance with 37 CFR 1.121(b) are required in reply to the Office action to avoid abandonment of the application. Any amended replacement drawing sheet should include all of the figures appearing on the immediate prior version of the sheet, even if only one figure is being amended. The replacement sheet(s) should be labeled "Replacement Sheet" in the page header (as per 37 CFR 1.84(c)) so as not to obstruct any portion of the drawing figures. If the changes are not accepted by the examiner, the applicant will be notified and informed of any required corrective action in the next Office action. The objection to the drawings will not be held in abeyance.

Specification

2. The disclosure is objected to because of the following informalities:

- Page 5, lines 16 – 17, there are discrepancies for the title description.
- Page 12, line 2, there is a typo. The term "3x4" should be corrected as "4x3" for 4 inputs and 3 outputs according to the drawing disclosed.

Appropriate correction is required.

Claim Rejections - 35 USC § 102

3. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

4. Claims 1, 2, 9, 12, 13, 20, 21, 24, are rejected under 35 U.S.C. 102(e) as being anticipated by Eng et al. (U.S. Patent No. 4955017).

Regarding claims 1, 12, 21, 24, Eng et al. discloses the limitation of an MxN packet switch for switching M input packets arriving in each of a sequence of frame times to N output ports (Abstract, lines 2 – 9), the switch comprising an input module, having M inputs and B outputs, B>M (column 1, lines 48 – 49), for switching the M input packets to M of the B outputs to produce M switched packets during each of the frame times (column 1, lines 49 – 59), a packet buffer including B registers, coupled to the input module (column 6, lines 44 – 46), for storing the M switched packets into M available registers during each of the frame times to produce M stored packets (column 6, lines 41 – 44), and an output module, having B inputs and N outputs coupled to the packet buffer (column 6, lines 60 – 66), for transferring up to N packets from occupied registers in each of the frame times to the output ports based upon destination addresses contained within each of the stored packets (column 2, lines 60 – 65; column

6, lines 66 – 68, column 7, lines 1 – 3).

Regarding claims 2, 13, Eng et al. discloses the limitation of the packet switch as recited in claim 1 wherein the input module is an MxB crossbar switch (column 1, lines 48 – 52), and the output module is a BxN crossbar switch (column 1, lines 53 – 59).

Regarding claims 9, 20, Eng et al. discloses the limitation of the packet switch as recited in claim 1 wherein each of the B registers is a circular shift register (column 7, lines 23 – 25).

Claim Rejections - 35 USC § 103

5. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

6. Claims 3 – 8, 10 – 11, 14 – 19, 22 – 23 are rejected under 35 U.S.C. 103(a) as being unpatentable over Eng et al. (U.S. Patent No. 4955017) in view of Holden (U.S. Patent No. 5583861).

Regarding claims 3, 14, Eng et al. discloses the limitation of an MxN packet switch for switching M input packets arriving in each of a sequence of frame times to N

output ports (Abstract, lines 2 – 9), Eng et al. does not disclose expressly the packet switch as recited in claim 1 wherein the packet buffer is a one-stop shared buffer memory. Holden discloses the limitation of the packet switch as recited in claim 1 wherein the packet buffer is a one-stop shared buffer memory (Abstract, lines 4 – 6). It would have been obvious to modify Eng et al. to include the packet switch as recited in claim 1 wherein the packet buffer is a one-stop shared buffer memory such as that taught by Holden in order to optimally uses available memory for queueing and buffering data packets at high-traffic crosspoints without slowing switching operations.

Regarding claims 4, 15, 22, Eng et al. discloses the limitation of an MxN packet switch for switching M input packets arriving in each of a sequence of frame times to N output ports (Abstract, lines 2 – 9), Eng et al. does not disclose expressly the packet switch as recited in claim 1 further including queues and their identifiers to store the destination addresses and wherein the output module transfers N_1 packets from the occupied registers in each of the frame times to N_2 output ports indicated by identifiers of the queues, $N_1 \leq N_2 \leq N$. Holden discloses the limitation of the packet switch as recited in claim 1 further including queues and their identifiers to store the destination addresses (column 6, lines 43 – 47; column 5, lines 39 – 43; column 2, lines 23 – 26) and wherein the output module transfers N_1 packets from the occupied registers in each of the frame times to N_2 output ports indicated by identifiers of the queues, $N_1 \leq N_2 \leq N$ (column 7, lines 1 – 2; lines 11 – 16). It would have been obvious to modify Eng et al.

to include a the packet switch as recited in claim 1 further including queues and their identifiers to store the destination addresses and wherein the output module transfers N_1 packets from the occupied registers in each of the frame times to N_2 output ports indicated by identifiers of the queues, $N_1 \leq N_2 \leq N$ such as that taught by Holden in order to optimally uses available memory for queueing and buffering data packets at high-traffic crosspoints without slowing switching operations.

Regarding claims 5, 16, Eng et al. discloses the limitation of an MxN packet switch for switching M input packets arriving in each of a sequence of frame times to N output ports (Abstract, lines 2 – 9), Eng et al. does not disclose expressly the packet switch as recited in claimed further including a register selector for assigning the M of the B registers during each of the frame times to generate M assigned registers. Holden discloses the limitation of the packet switch as recited in claimed further including a register selector for assigning the M of the B registers during each of the frame times to generate M assigned registers (column 5, lines 58 – 62; column 15, lines 24 – 26). It would have been obvious to modify Eng et al. to include a the packet switch as recited in claimed further including a register selector for assigning the M of the B registers during each of the frame times to generate M assigned registers such as that taught by Holden in order to optimally uses available memory for queueing and buffering data packets at high-traffic crosspoints without slowing switching operations.

Regarding claims 6, 17, Eng et al. discloses the limitation of an MxN packet

switch for switching M input packets arriving in each of a sequence of frame times to N output ports (Abstract, lines 2 – 9), Eng et al. does not disclose expressly the packet switch as recited in claim 5 further including M header hoppers, coupled to the input module, for storing header information from each of the M input packets in each of the frame times and M addresses of the M assigned registers for the M input packets in each of the frame times. Holden discloses the limitation of the packet switch as recited in claim 5 further including M header hoppers, coupled to the input module (column 5, lines 39 – 44; lines 58 – 62), for storing header information from each of the M input packets in each of the frame times and M addresses of the M assigned registers for the M input packets in each of the frame times (column 16, lines 32 – 40). It would have been obvious to modify Eng et al. to include a the packet switch as recited in claim 5 further including M header hoppers, coupled to the input module, for storing header information from each of the M input packets in each of the frame times and M addresses of the M assigned registers for the M input packets in each of the frame times such as that taught by Holden in order to optimally uses available memory for queueing and buffering data packets at high-traffic crosspoints without slowing switching operations.

Regarding claims 7, 18, Eng et al. discloses the limitation of an MxN packet switch for switching M input packets arriving in each of a sequence of frame times to N output ports (Abstract, lines 2 – 9), Eng et al. does not disclose expressly the packet switch as recited in claim 6 further including N queues for storing the addresses of the

assigned registers in each of the frame times as transmitted to the N queues from the M header hoppers based upon destination information in the header information of the packets. Holden discloses the limitation of the packet switch as recited in claim 6 further including N queues for storing the addresses of the assigned registers in each of the frame times as transmitted to the N queues from the M header hoppers based upon destination information in the header information of the packets (column 15, lines 24 – 39). It would have been obvious to modify Eng et al. to include a packet switch as recited in claim 6 further including N queues for storing the addresses of the assigned registers in each of the frame times as transmitted to the N queues from the M header hoppers based upon destination information in the header information of the packets such as that taught by Holden in order to optimally uses available memory for queueing and buffering data packets at high-traffic crosspoints without slowing switching operations.

Regarding claims 8, 11, 19, Eng et al. discloses the limitation of an MxN packet switch for switching M input packets arriving in each of a sequence of frame times to N output ports (Abstract, lines 2 – 9), Eng et al. does not disclose expressly the packet switch as recited in claim 7 wherein the header hoppers, the register selector, and the queues are coupled via a multi-user bus. Holden discloses the limitation of the packet switch as recited in claim 7 wherein the header hoppers, the register selector, and the queues are coupled via a multi-user bus (Fig. 5, element "Back pressure"; column 7, lines 33 – 35; column 9, lines 5 – 8). It would have been obvious to modify Eng et al. to

include a packet switch as recited in claim 7 wherein the header hoppers, the register selector, and the queues are coupled via a multi-user bus such as that taught by Holden in order to optimally uses available memory for queueing and buffering data packets at high-traffic crosspoints without slowing switching operations.

Regarding claims 10, 23, Eng et al. discloses the limitation of a MxN packet switch for switching M input packets arriving in each of a sequence of frame times to N output ports (Abstract, lines 2 – 9), the switch comprising a MxB input crossbar switch, B>M (column 1, lines 48 – 49), for switching the M input packets to M of the B outputs to produce M switched packets during each of the frame times (column 1, lines 49 – 59), a BxN output crossbar switch coupled to the packet buffer (column 6, lines 60 – 66), for transferring up to N packets from occupied registers in each of the frame times to the output ports based upon destination addresses(column 2, lines 60 – 65; column 6, lines 66 – 68, column 7, lines 1 – 3). Eng et al. does not disclose expressly a one-stop shared buffer memory, including B registers, coupled to the input crossbar switch, for storing the M switched packets into M available registers during each of the frame times to produce M stored packets, a register selector for assigning the M of the B registers during each of the frame times to generate M assigned registers, M header hoppers, coupled to the input crossbar switch, for storing header information from each of the M input packets in each of the frame times and M addresses of the M assigned registers for the M input packets in each of the frame times, and N queues for storing the addresses of the assigned registers in each of the frame times as transmitted to the N

queues from the M header hoppers based upon destination information in the header information. Holden discloses the limitation of a one-stop shared buffer memory (Abstract, lines 4 – 6), including B registers, coupled to the input crossbar switch, for storing the M switched packets into M available registers during each of the frame times to produce M stored packets (column 6, lines 41 – 44), a register selector for assigning the M of the B registers during each of the frame times to generate M assigned registers (column 5, lines 58 – 62; column 15, lines 24 – 26), M header hoppers, coupled to the input crossbar switch (column 5, lines 39 – 44; lines 58 – 62), for storing header information from each of the M input packets in each of the frame times and M addresses of the M assigned registers for the M input packets in each of the frame times (column 16, lines 32 – 40), and N queues for storing the addresses of the assigned registers in each of the frame times as transmitted to the N queues from the M header hoppers based upon destination information in the header information (column 15, lines 24 – 39). It would have been obvious to modify Eng et al. to include a one-stop shared buffer memory, including B registers, coupled to the input crossbar switch, for storing the M switched packets into M available registers during each of the frame times to produce M stored packets, a register selector for assigning the M of the B registers during each of the frame times to generate M assigned registers, M header hoppers, coupled to the input crossbar switch, for storing header information from each of the M input packets in each of the frame times and M addresses of the M assigned registers for the M input packets in each of the frame times, and N queues for storing the addresses of the assigned registers in each of the frame times as transmitted to the N

queues from the M header hoppers based upon destination information in the header information such as that taught by Holden in order to optimally uses available memory for queueing and buffering data packets at high-traffic crosspoints without slowing switching operations.

Conclusion

7. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Andrew C. Lee whose telephone number is (571) 272-3131. The examiner can normally be reached on Monday through Friday from 8:30am - 5:00pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Wellington Chin can be reached on (571) 272-3134. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Ajit Patel
Primary Examiner